Supporting Online Material for

**Oxide Nanoelectronics On Demand**
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Oxide Nanoelectronics on Demand:

Supporting Online Material

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Figure S1. (A) 5mm × 5mm optical image of patterned LaAlO3/SrTiO3 structure with nine electrode sets. (B) 50 μm × 50 μm AFM image showing ends of four Au electrodes and central writable area. (C) 1μm × 1μm AFM image showing (~3Å) terrace structure due to the substrate miscut.

The structure investigated here consists of nominally 3.3 unit cells (uc) of LaAlO3, grown by pulsed laser deposition at 780°C in an O2 pressure of 7.5×10⁻⁵ mbar on a TiO2-terminated insulating SrTiO3 substrate. The LaAlO3 growth was stopped after a number of laser pulses that correspond to the growth of 3.3 unit cells, as calibrated by the number of laser pulses that yield 3 unit cells. After growth, the sample was cooled in 400 mbar of
O$_2$ with a 1 hour oxidation step at 600°C. All measurements were carried out in air at 295 K. The sample was maintained in a dark environment to suppress carrier photoexcitation in SrTiO$_3$ (bandgap $E_g \sim 3.2$ eV). Sets of electrodes, consisting of four gold fingers that connect to macroscopic pads suitable for placing electrical contacts (Fig S1 (A)), form ohmic contacts with the interface due to the Ar-ion etching prior to the gold deposition. Between the ends of the four gold fingers is a 40 µm × 40 µm unetched area (Fig S1 (B)) where the devices are formed. A close-up AFM image (Fig S1 (C)) reveals a terrace structure, resulting from a slight miscut of the SrTiO$_3$ substrate.
Figure S2. For the SketchFET structure, source-drain current measured as a function of the tip position across the wire, while cutting the wire with the tip biased negatively. A sharp drop in conductance occurs when the tip passes the wire. The decrease in conductance can be fit to a profile \( I(x) = I_0 - I_1 \tanh(x/h) \). Also plotted is the deconvolved differential current \((dI/dx)^{-1}\). (A) Cutting a wider portion of the channel (written with 10 V) with -10 V tip bias, deconvolved differential current shows a full width at half maximum of \( \delta x = 12 \) nm. (B) Cutting narrower portion of the channel (written with 3 V) with -3 V tip bias, deconvolved differential current shows a full width at half maximum of \( \delta x = 2.1 \) nm. (C) Repeated cutting and restoring of a 12 nm nanowire using \( V_{tip} = \pm 10 \) V.
**Figure S3.** T-Junction. (A), I-V characteristic between source and drain (B) at different gate bias ($V_{GD} = -3 \, \text{V}, \, 0 \, \text{V}, \, 3 \, \text{V}$) is all linear. (C) Intensity plot of $I_D(V_{GD}, V_{SD})$. The behavior is well described by a simple resistive network.

**Figure S4.** (A) For the SketchFET structure, $I$-$V$ characteristic between source and drain (blue curve) is plotted together with $I$-$V$ characteristic between gate and drain (red curve). (B) For the Double-Tunnel junction structure, $I$-$V$ character between source 1 and drain (blue curve) is plotted together with $I$-$V$ character between source 2 and drain (red curve).
**Figure S5.** $I-V$ characteristics of a SketchFET with a larger barrier. Drain current $I_D$ is plotted as a function of source bias $V_{SD}$ at various gate biases $V_{GD}$, showing a more pronounced field effect.

**Frequency Response of SketchFET**

A small-amplitude ($V_{SO} \sim 100$ mV) sinusoidal bias signal $V_{SD}(t) = V_{SO \text{ }}\cos(\Omega t)$ is applied to the source. The gate signal is derived by amplitude modulating at a low frequency:

$\omega/2\pi = 1.248$ kHz: $V_{GD}(t) = \cos(\omega t)V_{SD}(t) = V_{SO} (\cos \Omega t + \cos \Omega t)$ where $\Omega = \Omega \pm \omega$.

The resulting drain current $I_D$ is measured by a lock-in amplifier at the reference frequency $\omega/2\pi$. Detection of a non-zero component of $I_D$ at frequency $\omega/2\pi$ arises due to signal mixing by the transistor, i.e.,

$I_D(t) \sim g(\Omega+)\cos(\Omega t)\cos(\Omega t) + g(\Omega)\cos(\Omega t)\cos(\Omega t) + I_{\Omega,\Omega+,\Omega-} = M(\Omega)\cos(\omega t) + \text{higher frequency terms.}$

The mixing strength $M$ characterizes the frequency response of the SketchFET.
Figure S6. (A) Schematic diagram of frequency response measurement. (B) Normalized frequency response of SketchFET and a commercial NPN small signal transistor (cut-off frequency is 900MHz) with no external resistor and resistor of 500 Ω, 10 kΩ, 1M Ω connected in series with the emitter.

The source-gate capacitance can be estimated from the cutoff frequency using

$$\frac{1}{f_T} = 2\pi R_S \left( C_{SG} + C_{DG} \right).$$

By measuring the I-V characteristic of a T-junction with 12 nm wide lead of same size as SketchFET (Fig S1), we estimate the typical value of the lead resistance $R_S = 1$ MΩ, together with $f_T = 5$ MHz, and obtain $C_{SG} \approx C_{DG} \approx 20$ fF. For comparison, we characterize a commercial NPN small signal transistor (Central Semiconductor Corp. 2N709A) with various resistances $R_e = 500 \, \Omega$, 10 kΩ and 1 MΩ connected in series with the emitter. This transistor has a specified $f_T$ of 900 MHz and collector-base capacitance $C_{cb,\text{spec}} = 3$ pF. By increasing $R_e$, $f_T$ drops monotonically, eventually scaling according to $f_T = (2\pi R_e C_{cb})^{-1}$. When $R_e = 1$ MΩ, $f_T$ is 20 kHz, calculated $C_{cb,\text{meas}} = 8$ pF in reasonably good agreement with the manufacturer’s specifications.
Figure S7. Power gain of SketchFET structure as a function of source bias $V_{SD}$ plotted for various values of the gate bias $V_{GD}$. 
Figure S8. (A) SketchFET performance over time under vacuum conditions (~10^{-5} Torr). Plotted are $I_D(V_{SD})$ for two different values of the gate bias $V_{GD} = 0$ V (blue) and $V_{GD} = 2$ V (red). (B) Time evolution of average conductance $\overline{G}_{SD} \equiv (I_D(2V) - I_D(-2V)) / 4V$ and fractional change in conductance induced by $V_{GD}$ 
$\Delta \overline{G}_{SD} = 100\% \left( \frac{\overline{G}_{SD}(V_{GD} = 2V) - \overline{G}_{SD}(V_{GD} = 0V)}{\overline{G}_{SD}(V_{GD} = 0V)} \right)$. The dashed line indicates the calculated conductance of the structure (channel and leads) based on a planar conductivity $\sigma_{film} \approx 5 \times 10^{-4}$ S.