Supplementary Materials for

1D-1D Coulomb Drag Signature of a Luttinger Liquid

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Published 23 January 2014 on Science Express
DOI: 10.1126/science.1244152

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Materials and methods
The vertically-integrated double quantum wires used in this Letter are patterned on a n-doped GaAs/AlGaAs electron bilayer heterostructure (wafer EA0975). The two 18 nm wide quantum wells are separated by a 15 nm wide Al$_{0.3}$Ga$_{0.7}$As barrier. The electron density is $1.1 \times 10^{11}$ cm$^{-2}$ for the upper (lower) 2DEG, yielding a combined mobility of $4.0 \times 10^5$ cm$^2$/V·s. Two sets of two split gates are deposited using electron beam lithography on the upper and the lower side of the sample using an epoxy-bound-and-stop-etch (EBASE) process. These gates define two wires that are $\sim 4.2 \ \mu$m long and $\sim 0.5 \ \mu$m wide. More details on the fabrication process is presented elsewhere (20). A schematics of the design used for the vertically-integrated quantum wires is presented in Fig. 1A, along with a SEM picture of a typical sample in Fig. 1C. From the typical vertical alignment uncertainty observed in our structures, the center-to-center interwire separation is bounded between 33 nm and 41 nm. The three samples used in this Letter (sample 2-L, 2-C and 3-R) were fabricated from the same heterostructure following identical processing steps. Sample 2-L and 3-R were both measured in a $^3$He refrigerator at temperature down to 330 mK and sample 2-C was measured in a dilution refrigerator with an electron temperature reaching down to $\sim 75$ mK. The measurements are performed using standard low frequency lock-in amplifier techniques. The conductance is measured using a two-wire measurements with an excitation voltage of 50 $\mu$V at a frequency of 9 Hz and the Coulomb drag measurements are performed sourcing a 4.5 nA current at a frequency of 9 Hz. Self consistency of the Coulomb drag measurement has also been verified (see (20) for more details).

The standard device operation goes as follow. First both the lower and the upper pinch-off gates (LPO and UPO) are adjusted such that they deplete the 2DEG closest to them without depleting significantly the 2DEG farthest from them. This allows for the suppression of 2D
tunnelling between the layers and to create independent contacts to each layer. These gates are then held at constant bias for the remainder of the Coulomb drag experiment. Following this, the bias applied to the plunger gates (LPL and UPL for the lower and upper plunger gates, respectively) is adjusted to create a single, independently contacted quantum wire in each layer. Since both plunger gates are capacitively coupled, sweeping the bias of a single gate affects the conductance of both quantum wires. Therefore, in a typical gate-voltage analysis experiment, the drag resistance is determined as a function of a single gate voltage (LPL in this report) while the other three gates are held at a fixed (negative) bias. A complete mapping of the drag resistance as a function of 1D subband occupancy can be obtained by performing successive LPL bias sweeps for all accessible UPL bias values, and these have published in an earlier report (20).